ABSTRACT

A method for testing semiconductor devices that output non-deterministic entity information such as packet and control signals is disclosed. The method includes the steps generating test signals with a semiconductor tester and applying the generated test signals to the device-under-test. Actual output entities from the DUT in response to the applied generated test signals are captured by the tester and compared to expected output entities. If a failure is identified in the comparing step, the method defines a window of valid expected entities and compares the failed actual output entity to the window of valid expected entities. If a match occurs between the failed actual output entity and any of the expected entities in the window, the actual entity is deemed valid.